

**FIG. 3**

FIG. 3  
cont)

FIG. 3D

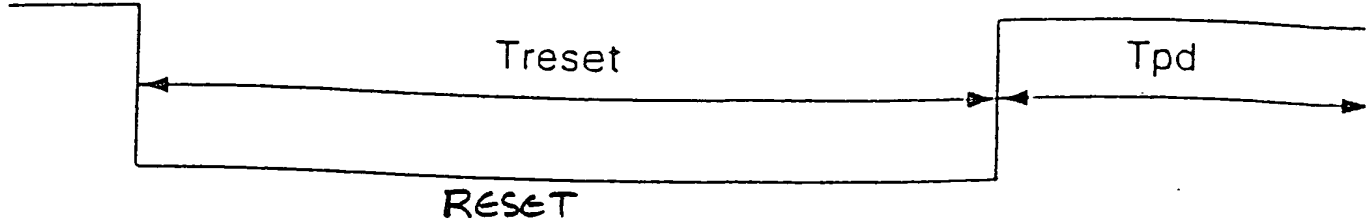


FIG. 3E

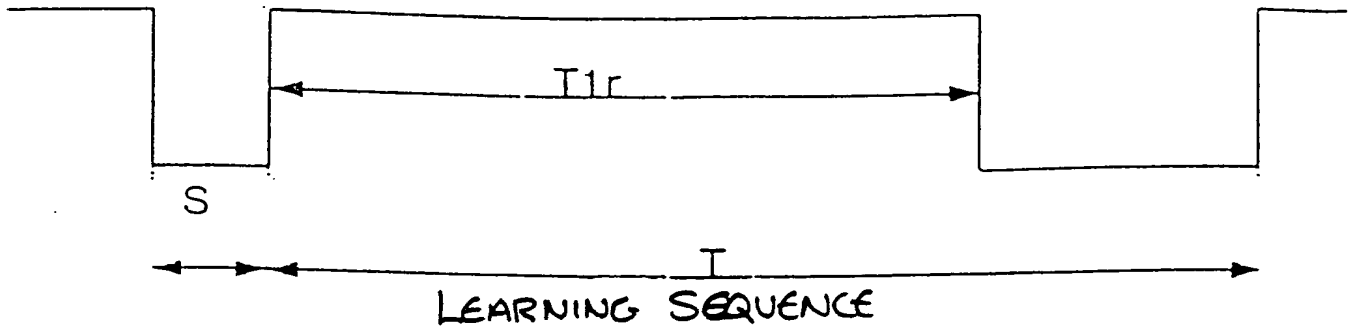


FIG. 3F

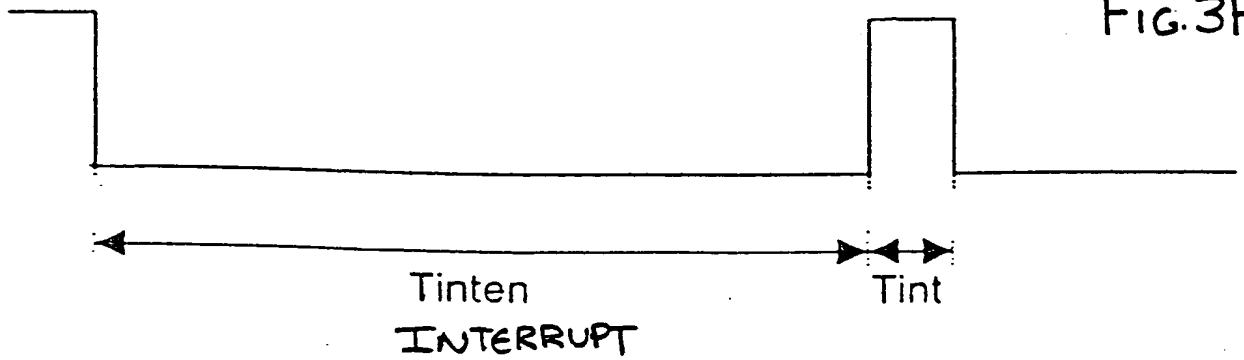


FIG. 5

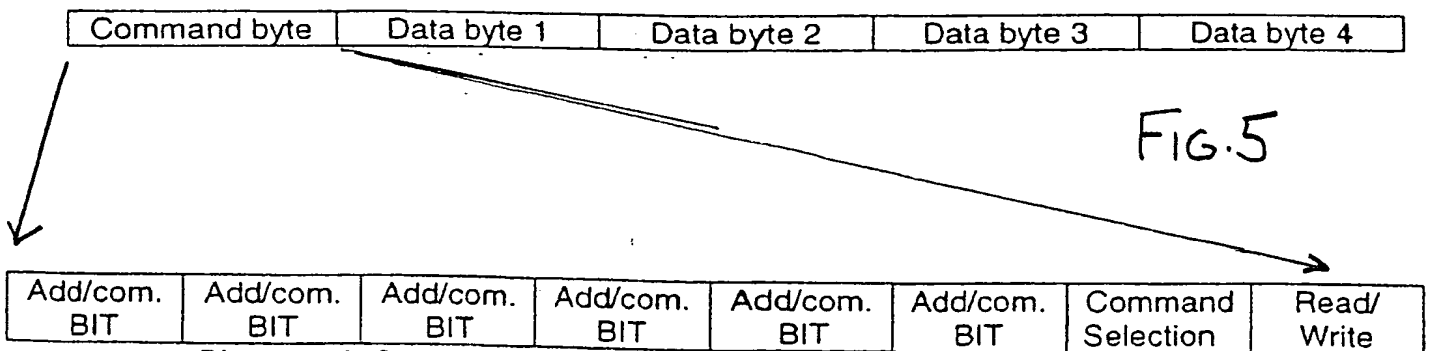
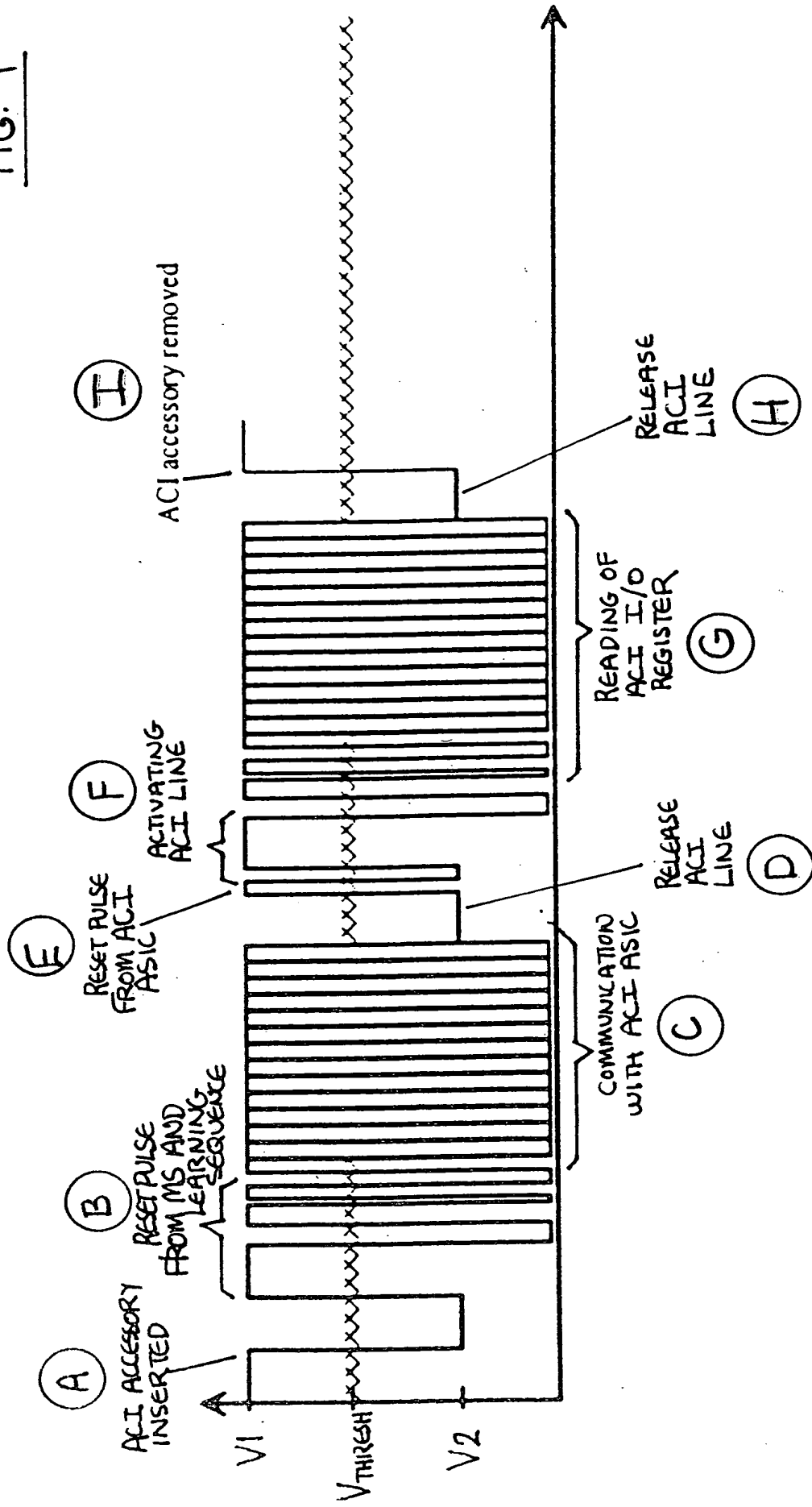


FIG. 4



The diagram shows the power supply voltage  $V_{cc}$  and its relationship to the threshold voltage  $V_{tresh}$  and the minimum operating voltage  $0.4 \cdot V_{cc}$ . The timing sequence includes:

- Sleep mode:** Initial state where  $V_{cc} < V_{tresh}$ .
- Active mode:** Triggered when  $V_{cc}$  rises above  $V_{tresh}$ . It includes a **Read** operation (shaded area) with timing parameters  $T_{pre}$  and  $T_r$ , and a **Write** operation (shaded area) with timing parameters  $T_{pre}$  and  $T_h$ .
- Sleep mode:** Occurs when  $V_{cc}$  falls below  $0.4 \cdot V_{cc}$ .

